REMARKS

Claims 19-30 were pending and were finally rejected. Claims 19, 22, 23, 25, and 29 have been amended. Based on amendments to claims and the following remarks, Applicants respectfully request reconsideration of the application.

Amendments to the Drawings

The Office Action indicates several potential informalities in the drawings. First, the Office Action indicates that Figure 4 contains a misspelled label "Scambler Polynomial." Second, the Office Action indicates that Figure 8 contains incorrect flow directions between elements 104 and 112 and between elements 116 and 108. Applicants were able to locate the version of the drawings to which the Examiner was referring, and apologize for their confusion. Figures 4 and 8 have now been updated to address the informalities identified by the Examiner.

Response to 35 U.S.C. § 112 Rejections

Claims 23, 24, and 30 were rejected under 35 U.S.C. § 112 as being indefinite. Claim 23 was rejected for insufficient antecedent basis for the limitation "the first array of de-scrambled output bits" and has been amended to refer instead to the "first array of de-scrambled packet bits." There is now sufficient antecedent basis for the limitation and Applicants request the rejection of claim 23 be withdrawn.

Claim 24 was rejected due to its dependence on claim 23. Because there is now sufficient antecedent basis for the limitation in claim 23, Applicants request the rejection of claim 24 also be withdrawn.

Claim 30 was rejected for insufficient antecedent basis for the limitation "the first de-scrambled output bits." Claim 29 has been amended to positively recite "to create first de-scrambled output bits" and now provides sufficient antecedent basis for the limitation in claim 30. Applicants request the rejection of claim 30 be withdrawn.

Response to 35 U.S.C. § 103(a) Rejections

Claims 19-30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Walker (U.S. Patent No. 6,862,701) in view of Suemura (U.S. App. Pub. 2001/0008001). This rejection is respectfully traversed.

Claims 19, 22, and 25 have been amended to more clearly present what is claimed. Claims 19, 22, and 25 require that scrambled bits be transmitted across a backplane from the scrambler to the switch fabric and then transmitted again from the switch fabric back across the backplane, in keeping with the teachings shown in Figure 8 (see, e.g., text "scrambler for backplane connectivity"). The transfer of the scrambled bits to the switch fabric is supported also by the specification, which states "the scrambler circuit 114 scrambles the array of packet bits before they are output by the ingress buffer manager 112 to a switch fabric 120." (page 7, lines 25-27) The retransmission of the scrambled bits by the switch fabric back across the backplane is further supported by the specification teaching "Controllers 122 determine the egress ports where the switch fabric 120 transfers the scrambled bits." (page 8, lines 1-2.) No new matter has been added by this amendment.

The Examiner stated that Walker fails to disclose scrambling packet bits received from the ingress circuit or a switch fabric. The Examiner asserts, however, that Suemera scrambles output bits across a reconfigurable switch fabric for transferring scrambled data between a plurality of ports. Applicants' position is that the way in which Suemera operates neither teaches nor suggests the claim elements agreed as missing from Walker, as the claims are presently constituted. Accordingly, Applicants respectfully submit that the combination of Walker and Suemera is insufficient to create a *prima facie* case of obviousness for the amended claims.

Suemera uses an optical switch that optically routes signals from input fibers to output fibers. (Suemera, paragraph 28.) Due to this configuration, Suemera's input and output interfaces are re-paired every frame, and must be synchronized to each other at each re-pairing. (*Id.*) The input interfaces 2.0-2.3 perform electro/optical conversion of scrambled signals and the output interfaces 4.0-4.3 perform optical/electrical conversion of those signals. (*Id.*, paragraphs 64-65; *see also* Figures 3 and 6 for details of the interfaces.) The intervening optical switch merely routes photons from the input interfaces to the output interfaces. Thus in this respect Suemera adds nothing to Walker—each scrambled signal passes over a single

communication link, albeit one that can be optically reconfigured between frames, before being descrambled.

Applicants could find no mention in Walker or Suemera of sending scrambled bits over a backplane and receiving them at a switch fabric port of a reconfigurable switch fabric for switching across the switch fabric, and then retransmitting the scrambled bits over the backplane from another switch fabric port, as required by claim 19. This infers that the switch fabric must maintain two separate switch fabric communication links, one coupled to the scrambler, and one coupled to the descrambler, across the backplane. This avoids the requirement of Suemera's optical approach that links be re-synchronized every frame, since the links across the backplane are links to the claimed switch fabric, not through a switch to each other. Note that Suemera does not teach receiving scrambled bits, transferring them, and retransmitting them—his optical switch merely routes light emanating from the ingress transmitters onto output fibers, with no attempt to receive or retransmit the bits represented by the photons.

Similar arguments apply to dependent claim 22, which adds the limitation of a descrambler that receives scrambled data over the backplane from the switch fabric—data that was received by the switch fabric from a scrambler communicating across a different backplane link. Likewise, method claim 25 also recites the two backplane transmissions.

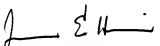
Applicants respectfully submit that Suemera and Walker, alone, or in combination, do not teach transferring bits "over the backplane" with a switch fabric as is claimed in claims 19, 22, and 25. Accordingly, Applicants request that the rejection of claims 19, 22, and 25 be withdrawn.

Claims 20-21, 23-24, and 26-30 are dependent claims that depend respectively from at least one of claims 19, 22, and 25. Based on the argument presented above for claims 19, 22, and 25, Applicants respectfully request that the rejection of claims 20-21, 23-24, and 26-30 also be withdrawn.

Conclusion

For the foregoing reasons, Applicants respectfully request allowance of claims 19-30 as presently constituted. The Examiner is encouraged to telephone the undersigned at 512.867.8502 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,



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I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office, via EFS-Web, on the date indicated below:

on Date January 19, 2007

Susan Lien

B

SCAMBLER POLYNOMIAL
OF 1+X(39)+X(58)

```
Dout[0:38]=NS[38:0]^NS[57:19]^Din[0:38];
Dout(0)=NS(38)^NS(57)^Din(0);
Dout(1)=NS(37)^NS(56)^Din(1);
Dout(2)=NS(36)^NS(55)^Din(2);
Dout(3)=NS(35)^NS(54)^Din(3);
Dout(4)=NS(34)^NS(53)^Din(4);
Dout(5)=NS(33)^NS(52)^Din(5);
Dout(6)=NS(32)^NS(51)^Din(6);
Dout(7)=NS(31)^NS(50)^Din(7);
Dout(8)=NS(30)^NS(49)^Din(8);
Dout(9)=NS(29)^NS(48)^Din(9);
Dout(10)=NS(28)^NS(47)^Din(10);
Dout(11)=NS(27)^NS(46)^Din(11);
Dout(12)=NS(26)^NS(45)^Din(12);
Dout(13)=NS(25)^NS(44)^Din(13);
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Dout(19)=NS(19)^NS(38)^Din(19);
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Dout(21)=NS(17)^NS(36)^Din(21);
Dout(22)=NS(16)^NS(35)^Din(22);
Dout(23)=NS(15)^NS(34)^Din(23);
Dout(24)=NS(14)^NS(33)^Din(24);
Dout(25)=NS(13)^NS(32)^Din(25);
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Dout(32)=NS(6)^NS(25)^Din(32);
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Dout(35)=NS(3)^NS(22)^Din(35);
Dout(36)=NS(2)^NS(21)^Din(36);
Dout(37)=NS(1)^NS(20)^Din(37);
Dout(38)=NS(0)^NS(19)^Din(38);
```

FIG.4

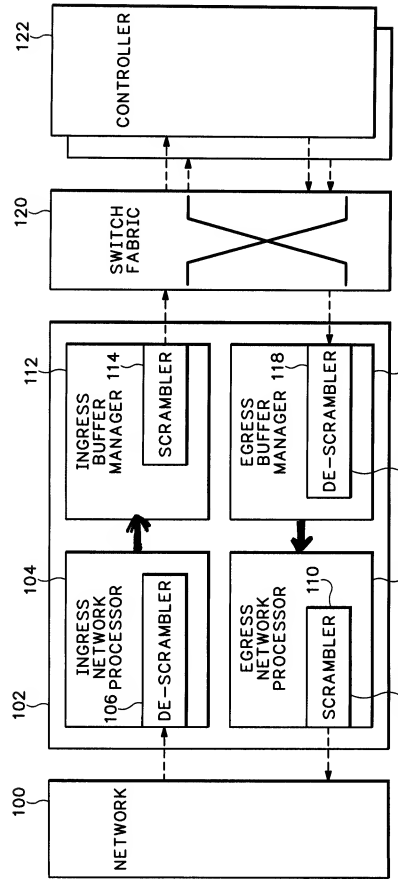
99
122
CONTROLLER
120
SWITCH FABRIC
112
INGRESS BUFFER MANAGER 114
SCRAMBLER
EGRESS BUFFER MANAGER 118
DE-SCRAMBLER
116
SCRAMBLER FOR BACK PLANE CONNECTIVITY
104
INGRESS NETWORK PROCESSOR 106
DE-SCRAMBLER
EGRESS NETWORK PROCESSOR
110
SCRAMBLER
108
SCRAMBLER FOR NETWORK INTERFACE
102
100
NETWORK

FIG.8